Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) An electron sensing device for receiving electrons from an output surface of an electron gain device, the electron sensing device comprising:

a silicon die including an active surface area for positioning below the output surface of an electron gain device,

wherein the silicon die includes~~ing~~ a silicon step formed below and surrounding the active surface area, and

a first array of bond pads formed on the silicon step for providing output signals from the silicon die,

wherein when the electron sensing device is positioned below the electron gain device, a tight vertical clearance is formed between the output surface of the electron gain device and the active surface area of the electron sensing device, and

an array of terminals disposed on a periphery of the active surface area of the silicon die, and

an array of conductive stripes extending between the array of terminals and the first array of bond pads,

wherein each conductive stripe includes an end terminating at the first array of bond pads positioned below another end terminating at the array of terminals.

2. (Original) The electron sensing device of claim 1 including

a ceramic carrier for holding the silicon die, and

a second array of bond pads disposed on the ceramic carrier for making electrical contacts to the first array of bond pads.

3. (Canceled)

4. (Original) The electron sensing device of claim 1 wherein

the tight vertical clearance includes a vertical spacing of less than 100 microns, and

a vertical spacing between the output surface of the electron gain device and the first array of bond pads is greater than the tight vertical clearance.

5. (Original) The electron sensing device of claim 1 having active sensors including one of complementary metal oxide semiconductor (CMOS) sensors, charge coupled device (CCD) sensors, electron bombarded CMOS (EBCMOS) sensors, EBCCD sensors, and avalanche photo detector (APD) sensors.

6. (Original) An electron sensing device for receiving electrons from an output surface of an electron gain device, the electron sensing device comprising:

a silicon die including an active surface area for positioning below the output surface of the electron gain device,

an array of terminals disposed on a periphery of the active surface area of the silicon die,

an array of conductive stripes extending horizontally from the array of terminals to a diced end wall of the silicon die and bending downwardly to extend along the diced end wall of the silicon die,

a ceramic carrier positioned below the silicon die, including a plurality of pins for providing input/output signals to/from the silicon die, and

electrical connections formed between the array of conductive stripes and the plurality of pins,

wherein when the electron sensing device is positioned below the electron gain device, a tight vertical clearance is formed between the output surface of the electron gain device and the active surface area of the electron sensing device.

7. (Original) The electron sensing device of claim 6 wherein

the electrical connections include solder balls for forming electrical contacts between the array of conductive stripes and the plurality of pins.

8. (Original) The electron sensing device of claim 6 wherein

the tight vertical clearance includes a vertical spacing of less than 100 microns.

9. (Original) The electron sensing device of claim 6 having active sensors including one of CMOS sensors, CCD sensors, electron bombarded CMOS (EBCMOS) sensors, EBCCD sensors and avalanche photo detector (APD) sensors.

10. (Original) An electron sensing device for receiving electrons from an output surface of an electron gain device, the electron sensing device comprising:

a silicon die including an active surface area for positioning below the output surface of the electron gain device,

an array of first bond pads disposed on a periphery of the active surface area of the silicon die,

a ceramic carrier positioned below the silicon die, including a second array of bond pads disposed on the ceramic carrier and arranged to surround the first array of bond pads, and

a flexible decal having first and second frame borders, including conductive stripes extending between the first and second frame borders,

wherein when the flexible decal is pressed onto the silicon die and the ceramic carrier, the conductive stripes form electrical connections between the first array of bond pads and the second array of bond pads.

11. (Original) The electron sensing device of claim 10 wherein when the electron sensing device is positioned below the electron gain device, a tight vertical clearance is formed between the output surface of the electron gain device and the active surface area of the electron sensing device.

12. (Original) The electron sensing device of claim 11 wherein the tight vertical clearance includes a vertical spacing of less than 100 microns.

13. (Original) The electron sensing device of claim 10 wherein the ceramic carrier includes a plurality of pins electrically connected to the second array of bond pads for providing an input/output signal interface.

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Currently Amended) A first integrated circuit (IC) having a first surface area disposed in close proximity to a second surface area of a second IC, the first and second surface areas providing signal transfer between the first IC and the second IC, the first IC comprising:

a silicon die including the first surface area for positioning below the second surface area of the second IC,

wherein the silicon die includesing a silicon step formed below and surrounding the first surface area, and

a first array of bond pads formed on the silicon step for providing signal transfer from the silicon die,

wherein when the first IC is positioned below the second IC, a tight vertical clearance is formed between the first surface area and the second surface area, and

an array of terminals disposed on a periphery of the active surface area of the silicon die, and

an array of conductive stripes extending between the array of terminals and the first array of bond pads,

wherein each conductive stripe includes an end terminating at the first array of bond pads positioned below another end terminating at the array of terminals.

23. (Original) The first IC of claim 22 including

a ceramic carrier for holding the silicon die, and

a second array of bond pads disposed on the ceramic carrier for making electrical contacts to the first array of bond pads.

24. (Canceled)

25. (Original) The first IC of claim 22 wherein

the tight vertical clearance includes a vertical spacing of less than 100 microns, and

a vertical spacing between the first surface area of the first IC and the first array of bond pads is greater than the tight vertical clearance.

26. (Original) A first integrated circuit (IC) having a first surface area disposed in close proximity to a second surface area of a second IC, the first and second surface areas providing signal transfer between the first IC and the second IC, the first IC comprising:

a silicon die including the first surface area for positioning below the second surface area of the second IC,

an array of first bond pads disposed on a periphery of the first surface area of the silicon die,

a ceramic carrier positioned below the silicon die, including a second array of bond pads disposed on the ceramic carrier and arranged to surround the first array of bond pads, and

a flexible decal having first and second frame borders, including conductive stripes extending between the first and second frame borders,

wherein when the flexible decal is pressed onto the silicon die and the ceramic carrier, the conductive stripes form electrical connections between the first array of bond pads and the second array of bond pads.

27. (Original) The first IC of claim 26 wherein when the first IC is positioned below the second IC, a tight vertical clearance is formed between the first surface area of the first IC and the second surface area of the second IC.

28. (Original) The electron sensing device of claim 27 wherein the tight vertical clearance includes a vertical spacing of less than 100 microns.

29. (Original) The electron sensing device of claim 26 wherein the ceramic carrier includes a plurality of pins electrically connected to the second array of bond pads for providing an input/output signal interface.